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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/722,397	11/28/2003	Hiroki Mouri	2003-1721A	7183

513 7590 04/20/2007

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EXAMINER	
GIESY, ADAM	
ART UNIT	**PAPER NUMBER**
2627	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,397	MOURI ET AL.	
	Examiner	Art Unit	
	Adam R. Giesy	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *6-19,21 and 22* is/are allowed.

6)☒ Claim(s) *4,5 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida (US Pat. No. 6,377,525 B1) in view of Pupalaikis (US Pat. No. 6,701,335 B2) and further in view of Fischer et al. (hereinafter Fischer – US Pat. No. 6,167,415).

Regarding claim 4, Iida discloses a wobble signal processing apparatus comprising: a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal, and a RF signal (Figure 9, element 30); a WBL binarization circuit for smoothing edges of a wobble binary signal outputted from said pickup (Figure 10, element 345); a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup (Figure 9, element 32); an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal (Figure 10, element 342); an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC (Figure 9, element 34); a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal that is outputted from said pickup (Figure 10, element 341); a phase control circuit for

controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data (Figure 10, element 348); and a PLL (Phase Locked Loop) circuit which is connected to the phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit (Figure 10, element 341); wherein said address detection circuit and said waveform shaping circuit are digitally configured (see column 12, lines 1-5 – note that the ATIP decoder is constituted by a digital signal processor unit and is considered to be digitally configured); wherein said waveform shaping circuit includes a BPF (Band Pass Filter) as a digital filter (Figure 10, element 341). Iida does not disclose that the digital filter is constituted by an IIR digital filter including a reset function or that the digital filter calculates the optimum tap coefficients and stores them.

Pupalaikis discloses a filtering adjustment system that includes a band pass filter that is implemented with an IIR (Infinity Impulse Response) filter (column 3, lines 30-34). Pupalaikis further discloses that the IIR filter coefficients are calculated and stored in a library (external storage unit) until they are implemented (see column 9, line 22 thru column 10, line 5).

Furthermore, Fischer discloses a digital IIR filter with a reset function (see abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the wobble signal processing apparatus as disclosed by Iida with the band pass filter and infinity impulse response filter as disclosed by

Pupalaikis and the IIR filter with reset function as disclosed by Fischer, the motivation being to allow for a more robust and adjustable digital filtering scheme for a wobble signal circuit.

3. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida (US Pat. No. 6,377,525 B1) in view of Asano et al. (hereinafter Asano – US Pat. No. 6,621,772 B2).

Regarding claim 5, Iida discloses a wobble signal processing apparatus comprising: a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal, and a RF signal (Figure 9, element 30); a WBL binarization circuit for smoothing edges of a wobble binary signal outputted from said pickup (Figure 10, element 345); a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup (Figure 9, element 32); an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal (Figure 10, element 342); an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC (Figure 9, element 34); a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal that is outputted from said pickup (Figure 10, element 341); a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data (Figure 10, element 348); and a

PLL (Phase Locked Loop) circuit which is connected to the phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit (Figure 10, element 341); wherein said address detection circuit and said waveform shaping circuit are digitally configured (see column 12, lines 1-5 – note that the ATIP decoder is constituted by a digital signal processor unit and is considered to be digitally configured); wherein said address detection circuit comprises: a digital filter for filtering the digital signal outputted from said ADC (see column 12, lines 1-5). Iida does not disclose a PRML circuit.

Asano discloses an apparatus for reproducing optical discs that filters the reproduced signal in order to better acquire the wobble signal wherein the apparatus comprises a filter at the output of the ADC (Figure 76, element 584); and a PRML circuit for correcting errors in the signal outputted from the digital filter and detecting the ADIP signal by using the corrected signal (Figure 76, element 585).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the wobble signal processing apparatus as disclosed by Iida with the filtering and PRML circuits as disclosed by Asano, the motivation being to better filter out noise and other errors from the wobble signal.

4. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iida (US Pat. No. 6,377,525 B1) in view of Pupalaikis (US Pat. No. 6,701,335 B2) and further in view of Fischer et al. (hereinafter Fischer – US Pat. No. 6,167,415) and even further in view of Asano et al. (hereinafter Asano – US Pat. No. 6,621,772 B2).

Regarding claim 20, Iida discloses a wobble signal processing apparatus comprising: a pickup for reading information recorded on an optical disc medium on/from which data can be recorded/reproduced, and outputting a wobble binary signal, a wobble signal, and a RF signal (Figure 9, element 30); a WBL binarization circuit for smoothing edges of a wobble binary signal outputted from said pickup (Figure 10, element 345); a FEP (Front End Processor) for performing band limitation and gain control to the wobble signal outputted from said pickup (Figure 9, element 32); an ADC (Analog-to-Digital Converter) for converting the wobble signal outputted from said FEP into a digital signal (Figure 10, element 342); an address detection circuit for detecting an ADIP (Address In Pre-Groove) signal as address information of the data based on the digital signal outputted from said ADC (Figure 9, element 34); a waveform shaping circuit for generating a wobble binary signal waveform based on the RF signal that is outputted from said pickup (Figure 10, element 341); a phase control circuit for controlling the phase of the wobble binary signal outputted from said WBL binarization circuit with reference to the wobble binary signal waveform generated by said waveform shaping circuit, and outputting phase controlled data (Figure 10, element 348); and a PLL (Phase Locked Loop) circuit which is connected to the phase control circuit, for generating a sync clock based on the phase controlled data outputted from said phase control circuit (Figure 10, element 341); wherein said address detection circuit and said waveform shaping circuit are digitally configured (see column 12, lines 1-5 – note that the ATIP decoder is constituted by a digital signal processor unit and is considered to be digitally configured). Iida does not disclose low-pass filters or that the digital filter is

constituted by an IIR digital filter including a reset function or that the digital filter calculates the optimum tap coefficients and stores them.

Asano discloses an apparatus for reproducing optical discs that filters the reproduced signal in order to better acquire the wobble signal wherein the apparatus comprises an optical head, an amplifier circuit, an address detecting circuit and a low-pass filter circuit (Figure 76, element 579). Asano does not disclose that the low-pass filter is an IIR filter.

Pupalaikis discloses a filtering adjustment system that includes filtering with an IIR (Infinity Impulse Response) filter (column 9, lines 25-28).

Furthermore, Fischer discloses a digital IIR filter with a reset function (see abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the wobble signal processing apparatus as disclosed by Iida with the band pass filter and infinity impulse response filter as disclosed by Pupalaikis, the the low-pass filter as disclosed by Asano, and the IIR filter with reset function as disclosed by Fischer, the motivation being to further and more effectively limit high frequency noise that might appear in the wobble signal and allow for a more robust and adjustable digital filtering scheme for a wobble signal circuit.

Allowable Subject Matter

5. Claims 6-19, 21, and 22 are allowed over the prior art of record for the reasons stated in the previous Office Action, mailed on 8/23/2006.

Response to Arguments

6. Applicant's arguments with respect to claims 4, 5, and 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adam R. Giesy whose telephone number is (571) 272-7555. The examiner can normally be reached on 8:00am- 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William R. Korzuch can be reached on (571) 272-7589. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ARG 4/12/2007

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